AMENDMENTS TO THE CLAIMS

1-20. (Canceled)

21. (Currently Amended) A pulse generator circuit for generating an input signal for a flip flop circuit from a clock signal and from a data signal, comprising:

a clock pulse field effect transistor, at the gate terminal of which the clock signal is applied and at the first source/drain terminal of which the input signal for the flip flop circuit is provided;

a logic field effect transistor, at the gate terminal of which the data signal is applied and the first source/drain terminal of which is coupled to the second source/drain terminal of the clock pulse field effect transistor;

a feedback field effect transistor, at the gate terminal of which a feedback signal based on the clock signal is applied, the first source/drain terminal of which is coupled to the second source/drain terminal of the logic field effect transistor and at the second source/drain terminal of which a first electrical reference potential is applied, wherein the feedback field effect transistor is activated by a level of the clock signal that deactivates the clock pulse field effect transistor; and

a control unit configured to apply the data signal to the gate terminal of ~~control the clock pulse field effect transistor,~~ the logic field effect transistor before the clock signal is switched to a level that activates the clock pulse field effect transistor~~and the feedback field effect transistor~~ such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated.

22. (Previously Presented) The pulse generator circuit as claimed in claim 21, further comprising an additional clock pulse field effect transistor, at the gate terminal of which the clock signal is applied, at the first source/drain terminal of which a second electrical reference potential is applied, and the second source/drain terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor.

23. (Currently Amended) The pulse generator circuit as claimed in claim 22, further comprising

an additional feedback field effect transistor, the gate terminal of which is coupled to the gate terminal of the feedback field effect transistor, at the first source/drain terminal of which the second electrical reference potential is applied, and the second source/drain terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor, wherein the additional feedback field effect transistor is activated by a level of the clock signal that deactivates the clock pulse field effect transistor.

24. (Previously Presented) The pulse generator circuit as claimed in claim 21, comprising a bypass field effect transistor, the gate terminal of which is coupled to the flip flop circuit, at the first source/drain terminal of which the first electrical reference potential is applied, and the second source/drain terminal of which is coupled to the second source/drain terminal of the clock pulse field effect transistor.

25. (Canceled)

26. (Previously Presented) The pulse generator circuit as claimed in claim 22, wherein the first electrical reference potential is an electrical ground potential and/or wherein the second electrical reference potential is an electrical supply potential.

27. (Previously Presented) The pulse generator circuit as claimed in claim 21, wherein the clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor are field effect transistors of the n-type of conduction.

28. (Previously Presented) The pulse generator circuit as claimed in claim 23, wherein the additional clock pulse field effect transistor and the additional feedback field effect transistor are field effect transistors of the p-type of conduction.

29. (Previously Presented) The pulse generator circuit as claimed in claim 24, wherein the bypass field effect transistor is a field effect transistor of the n-type of conduction.

30. (Previously Presented) The pulse generator circuit as claimed in claim 21, wherein the clock pulse field effect transistor, the logic field effect transistor, and the feedback field effect transistor form a first signal path, and

wherein the pulse generator circuit further comprises a second signal path having a complementary clock pulse field effect transistor, a complementary logic field effect transistor, and a complementary feedback field effect transistor which are interconnected in a same way as the clock pulse field effect transistor, the logic field effect transistor, and the feedback field effect transistor of the first signal path, and the complementary clock pulse field effect transistor, the complementary logic field effect transistor, and the complementary feedback field effect transistor are interconnected for generating from the clock signal and from a complementary data signal which is complementary to the data signal a complementary input signal which is complementary to the input signal for the flip flop circuit.

31. (Previously Presented) The pulse generator circuit as claimed in claim 30, wherein the first source/drain terminal of the additional clock pulse field effect transistor of the second signal path is coupled to the gate terminal of the additional feedback field effect transistor of the first data path.

32. (Previously Presented) The pulse generator circuit as claimed in claim 30, wherein the first source/drain terminal of the clock pulse field effect transistor of the first signal path is coupled to the gate terminal of the additional feedback field effect transistor of the second data path.

33. (Canceled)

34. (Previously Presented) A circuit arrangement, comprising:

a pulse generator circuit as claimed in claim 21,

wherein the flip flop circuit, which is interconnected with the pulse generator circuit such that the input signal which is generated by the pulse generator circuit is coupled into the flip flop circuit.

35. (Previously Presented) The circuit arrangement as claimed in claim 34, wherein the flip flop circuit has storage field effect transistors configured to store a storage signal based on at least one of the input signal and the complementary input signal.

36. (Previously Presented) The circuit arrangement as claimed in claim 35, wherein the flip flop circuit comprises switching field effect transistors which are connected between the storage field effect transistors and the pulse generator circuit.

37. (Previously Presented) The circuit arrangement as claimed in claim 36, wherein the switching field effect transistors comprise a first switching field effect transistor, the gate terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor, at the first source/drain terminal of which the second electrical reference potential is applied, and the second source/drain terminal of which is coupled to a storage node of the storage field effect transistors.

38. (Previously Presented) The circuit arrangement as claimed in claim 37, wherein the switching field effect transistors comprise a second switching field effect transistor, the gate terminal of which is coupled to a gate terminal of a complementary bypass field effect transistor, at the first source/drain terminal of which the first electrical reference potential is applied, and the second source/drain terminal of which is coupled to the second source/drain terminal of the first switching field effect transistor.

39. (Previously Presented) The circuit arrangement as claimed in claim 38, wherein the flip flop circuit comprises a protective field effect transistor, the gate terminal of which is coupled to the gate terminal of the first switching field effect transistor, the first source/drain terminal of which is coupled to the second source/drain terminal of the first switching field effect transistor and to a source/drain terminal of a storage field effect transistor, and the second source/drain terminal of which is coupled to a source/drain terminal of another storage field effect transistor.

40. (Previously Presented) The circuit arrangement as claimed in claim 35, wherein the flip flop circuit has complementary storage field effect transistors configured to store a complementary storage signal which is complementary to the storage signal.

41. (Currently Amended) A circuit arrangement, comprising:

a pulse generator means for generating an input signal for a flip flop circuit from a clock signal and from a data signal, comprising:

a clock pulse field effect transistor, at the gate terminal of which the clock signal is applied and at the first source/drain terminal of which the input signal for a flip flop circuit is provided;

a logic field effect transistor, at the gate terminal of which the data signal is applied and the first source/drain terminal of which is coupled to the second source/drain terminal of the clock pulse field effect transistor;

a feedback field effect transistor, at the gate terminal of which a feedback signal based on the clock signal is applied, the first source/drain terminal of which is coupled to the second source/drain terminal of the logic field effect transistor and at the second source/drain terminal of which a first electrical reference potential is applied, wherein the feedback field effect transistor is activated by a level of the clock signal that deactivates the clock pulse field effect transistor; and

a control means for applying the data signal to the gate terminal of~~controlling the clock pulse field effect transistor,~~ the logic field effect transistor before the clock signal is switched to a level that activates the clock pulse field effect transistor~~and the feedback field effect transistor~~ such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated,

wherein the flip flop circuit is interconnected with the pulse generator means such that the input signal which is generated by the pulse generator circuit is coupled into the flip flop circuit.

42. (Currently Amended) A pulse generator circuit for generating an input signal for a flip flop circuit from a clock signal and from a data signal, comprising:

a clock pulse field effect transistor;

a logic field effect transistor;

a feedback field effect transistor; and

a control unit configured to apply the data signal to the gate terminal of ~~control the clock pulse field effect transistor,~~ the logic field effect transistor before the clock signal is switched to a level that activates the clock pulse field effect transistor ~~and the feedback field effect transistor~~ such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated.

43. (Currently Amended) A pulse generator circuit for generating an input signal for a flip flop circuit from a clock signal and from a data signal, comprising:

a clock pulse field effect transistor;

a logic field effect transistor;

a feedback field effect transistor; and

a control means for applying the data signal to the gate terminal of ~~controlling the clock pulse field effect transistor,~~ the logic field effect transistor before the clock signal is switched to a level that activates the clock pulse field effect transistor ~~and the feedback field effect transistor~~ such that, to generate the input signal, the clock pulse field effect transistor is chronologically activated after the logic field effect transistor and the feedback field effect transistor are activated.